Design of Logic Gates Using CNTFETs

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***Abstract*— Carbon Nanotube (CNT) is one of the emerging nano technology, which is showing high efficiency and it has wide range of applications in many different streams. The properties of Carbon Nano Tube Field Effect Transistors (CNTFETs) have been studied and are observed to be the promising candidate for the integrated circuit (IC) devices. These are widely studied as possible successors to silicon MOSFETs. In this paper the standard model has been designed for, MOSFET-like CNTFET devices. Various logic gates were designed using CNTFETs; their delays are obtained and compared with CMOS. Hspice simulations have been performed on various logic gates that are designed using the modeled CNTFET.**

***Index Terms*— Carbon Nanotube, Carbon Nanotube Field Effect Transistor, modelling, Logic gates.**

I. INTRODUCTION

As CMOS scales deeper into the nanoscale technology, various non idealities cause the device I-V characteristics to be substantially different from well-tempered MOSFETs. For example, the Source/Drain series resistance is now a significant component of the total ON-resistance. The metal contact (Schottky) source/drain UTB SOI FET also alters the I-V characteristics significantly. Novel non-Silicon devices such as CNFETs operate with completely different device physics with quasi-ballistic transport in the channel and Schottky barriers at the source/drain contacts [1]. These CNTFETs are expected to sustain the transistor scalability while increasing its performance. The major difference between CNTFETs and MOSFETs is that, the channel in CNTFET is formed by Carbon Nano Tubes instead of silicon. This enables a higher drive current density due to the large current carrier mobility compared to bulk silicon.

In this paper, section II Introduces the Carbon nanotubes, section III delves into the CNTFET and modeling aspects of CNTFET. Section IV deals with the Simulation results of basic logic gates. Sections V discuss the conclusion and future scope.

II. CARBON NANOTUBE (CNT)

Carbon is a Group 14 element that resides above silicon in the Periodic Table. Like silicon and germanium, carbon has four electrons in its valence shell. When carbon atoms are arranged in crystalline structures composed of hexagonal benzene-like rings, they from a number of allotropes that offer exceptional electrical properties. In semiconducting forms, these carbon nonmaterial's exhibit room-temperature mobilities over ten times greater than silicon. In addition, they can be scaled to smaller feature sizes than silicon while maintaining their electrical properties.

Carbon nanotubes were discovered by S. Ijiima in 1991 [2] while performing some experiments on molecular structure composed of carbonium. CNTs are hollow cylinders composed of one or more concentric layers of carbon atoms in a honey comb lattice arrangement. It can be classified into SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube).

The way that graphene is rolled is described by a pair of indices (n, m), which are called "chiral vector". Based on the chiral vector, it can be determined whether it's a metallic or semiconducting CNT as shown in Figure 2.

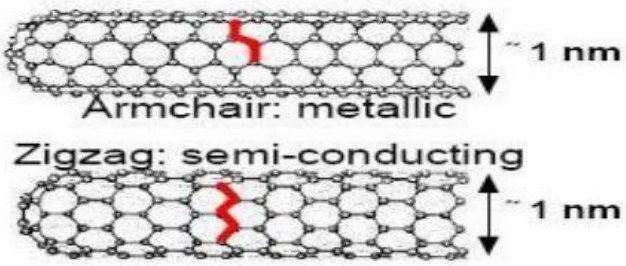


Fig.1: metallic and semiconducting CNT

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

A silicon wafer is covered with a thick silicon-dioxide film and then is fabricated using gold or platinum electrodes in standard semiconductor manufacturing process. A carbon nanotube is then introduced as a channel between source and drain terminals [3]. The underlying silicon wafer, heavily doped with impurities makes it a good conductor which serves as gate terminal. Applying the appropriate voltage to gate the nanotube is either on or off. The first carbon nanotube field-effect transistors (CNTFETs) were reported in 1998, figure 2 depicts the structure of CNTFET. There are several types of CNTFETs, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFET.

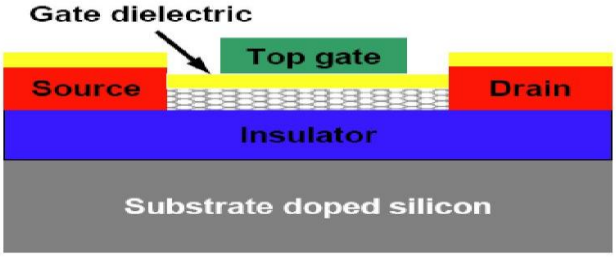


Fig.2: structure of CNTFET

In terms of the device operation, CNFET can be categorized as Schottky Barrier (SB) controlled FET (SB-CNFET) or

MOSFET-like FET [4]. The conductivity of SB-CNFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and the device performance of SB-CNFET is determined by the contact resistance. This is due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance. This SB-CNFET shows ambipolar behavior. Unlike SB-CNFET, MOSFET-like CNFET exhibits unipolar behavior either by suppressing electron (pFET) or hole (nFET) transport with heavily doped source/drain.

A model for nanoscale devices and circuits [5], is developed using both CMOS technology and carbon nanotube field effect transistors (CNFETs). This model provides large device speed improvement (6×for nFET and 14×for pFET) of CNFET over CMOS technology. The quasi-1D structure provides better electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI). Figure 3 depicts the MOSFET-like CNFET device structure.

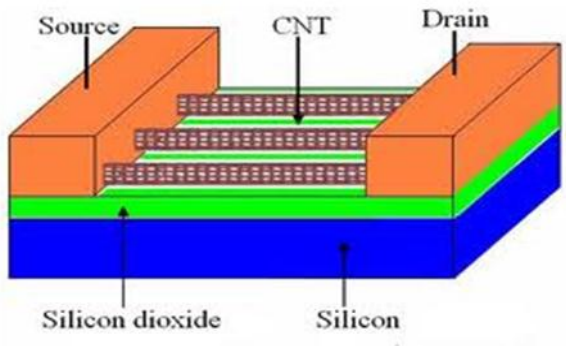


Fig.3: The 3-D structure of MOSFET like CNFETs with multiple channels

The complete CNFET device model [6] is implemented hierarchically in three levels. Device non-idealities are included hierarchically at each level. Level 1, models the intrinsic behavior of MOSFET-like CNFET. The level 2, models the device non-idealities: capacitance and resistance of the doped S/D CNT region as well as the possible Schottky Barrier (SB) resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, i.e. level 3 models the interface between CNFET device and CNFET circuits. This level deals with multiple CNTs per device, and includes the parasitic gate capacitance and screening due to adjacent CNTs.

IV. SIMULATION RESULTS

This model is designed for unipolar MOSFET like CNTFET devices, where each device may have one or more carbon nanotube. 32nm technology (19,0) semiconducting with 1.5nm diameter CNT is used . The supply voltage (VDD) given is 0.9V. The gate and drain voltage can be varied up to supply voltage. Figure 4, 5 shows current voltage characteristics of CNT model. Gate voltage starting from zero is varied up to supply voltage with a variation of"0.01 x supply". Curves for various values of Vdd with a variation of 0.1 x supply are shown.

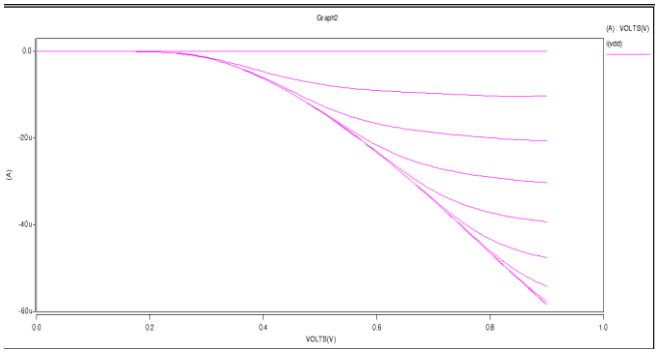


Fig.4: N channel CNT

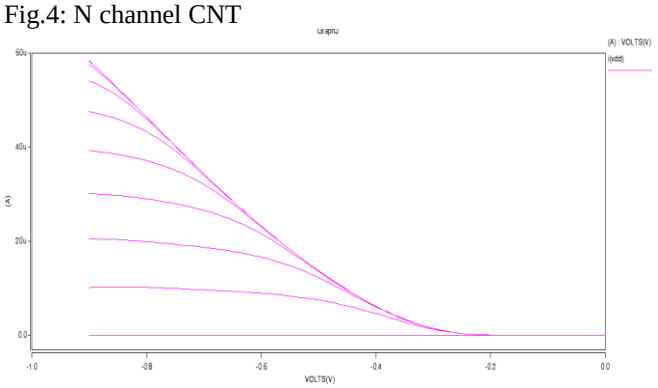
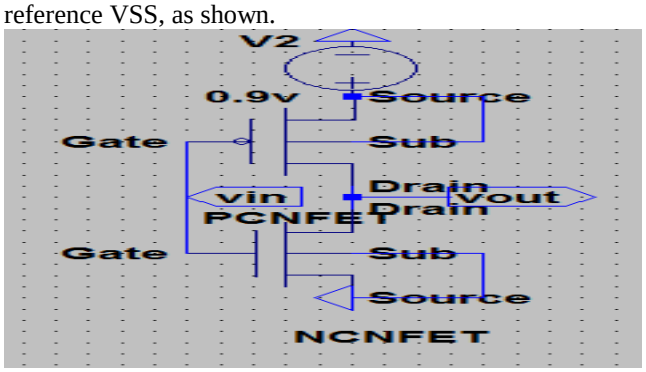


Fig.5: P channel CNT

Figure 6 shows an inverter consisting of P-type and N-type CNTFETs. The drain of pcnfet is coupled with the drain of ncnfet between a high supply voltage VDD and a low supply reference VSS, as shown.



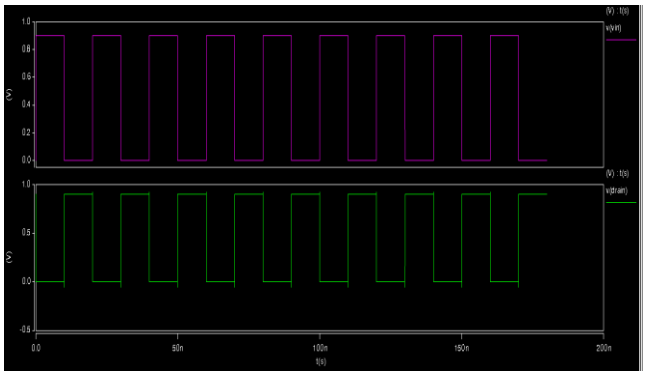
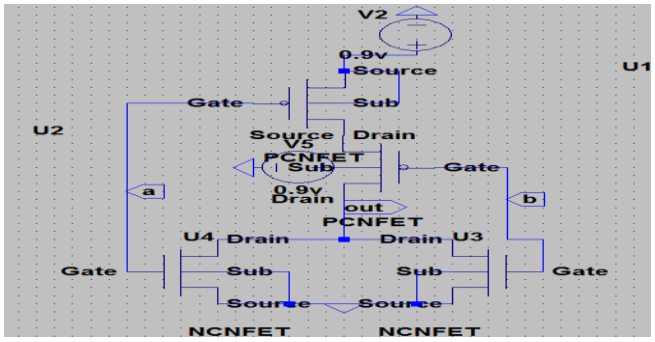


Fig 6: NOT gate behavior for CNTFET

Figure 7 shows NOR gate comprising of CNTFETs. It mainly consists of 2 pfets connected in series and 2 nfets connected in parallel between the supply and ground terminals.



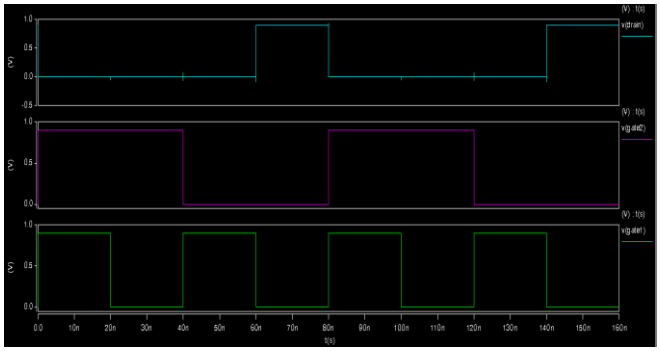
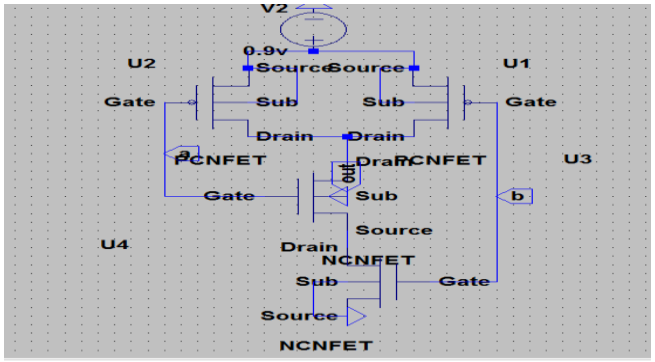


Fig 7: NOR gate behavior for CNTFET

Figure 8 shows NAND gate comprising of CNTFETs. It mainly consists of 2 pfets connected in parallel, 2 nfets connected in series. Both are coupled between the supply voltage and ground.



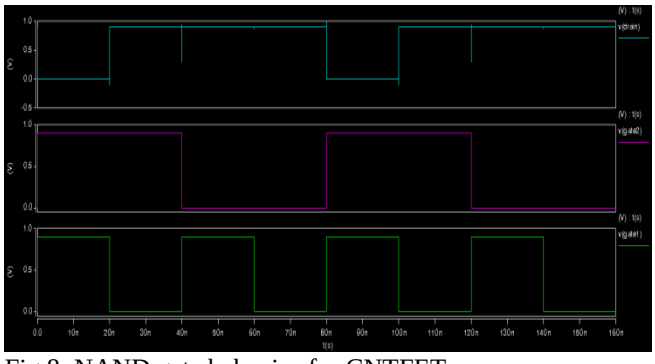
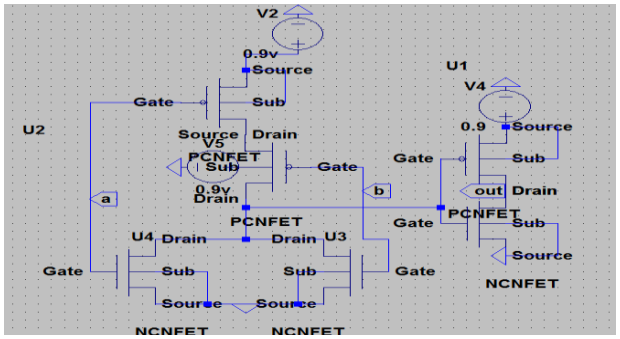


Fig 8: NAND gate behavior for CNTFET

Figure 9 shows or gate comprising of P-type and N-type CNTFETs. The P-type CNTFETs are placed in series between high supply reference VDD and N-type CNTFETs are placed in parallel, which is coupled to ground terminal, as shown.



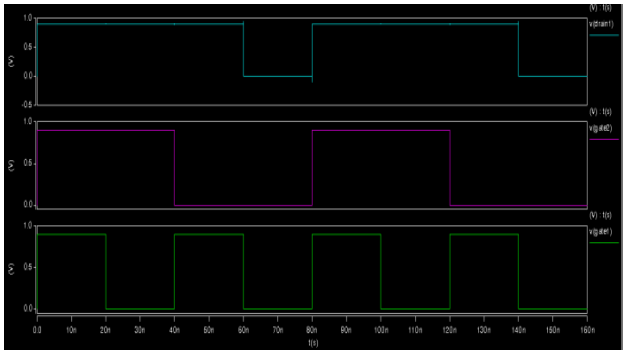
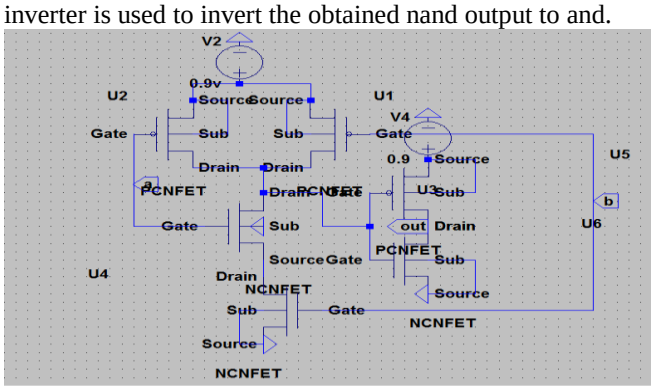


Fig 9: OR gate behavior for CNTFET

Figure 10 shows AND gate comprising of CNTFETs. It consists of driver PCNTFETs coupled together in Parallel between a high supply reference VDD and a Series active load transistors, which is coupled to ground terminal as shown. An inverter is used to invert the obtained nand output to and.



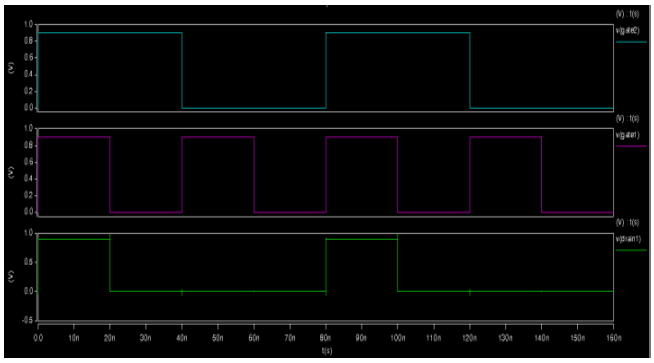


Fig 10 AND gate behavior for CNTFET

Figure 11 shows XOR gate comprising of CNTFETs. It comprises of driver PCNFETs coupled together in pull up network and NCNFETs in pull down circuits. This pull up network is connected between supply reference VDD and a series active load transistors, which is coupled to a low supply reference VSS as shown

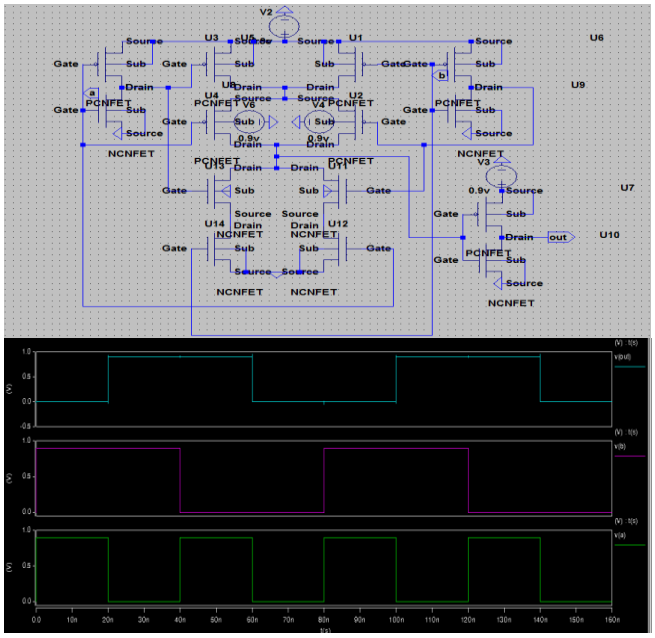


Fig 11: Structure of CNTFET XOR Gate and its behavior

Figure 12 shows XNOR gate comprising of CNTFETs. It comprises of driver CNTFETs coupled together in parallel between a high supply reference VDD and a series active load transistors, which is coupled to a low supply reference VSS as shown

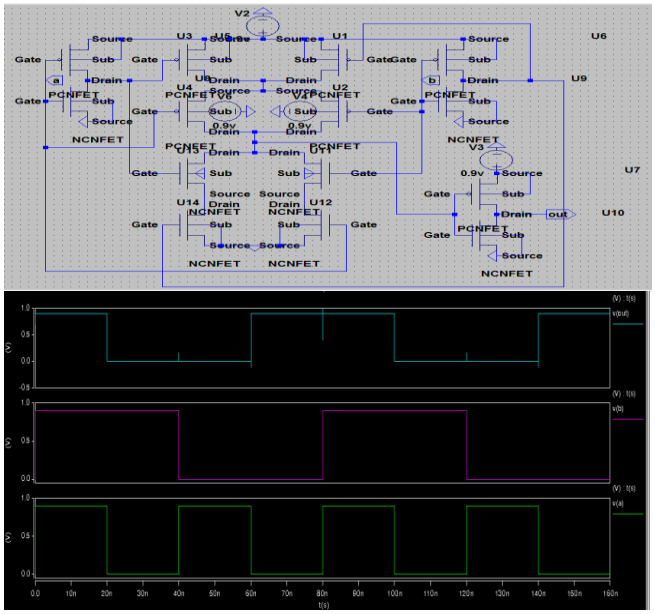


Fig 12: XNOR gate behavior for CNTFET

V. COMPARISION OF CNTFET WITH FINFETS

Table 1: Delay comparison with FinFETs

	CNTFET	FINFET
Inverter	5.07E-12	1.30E-11
Nand	2.55E-09	9.99E-09
Nor	2.91E-09	1.00E-08
And	1.00E-08	3.00E-08
Or	1.02E-08	3.84E-08
Xor	1.46E-11	1.68E-11
Xnor	2.03E-08	8.62E-11

VI. ONCLUSION AND FUTURE SCOPE

This paper adequately explains the various modeling aspects of the proposed CNTFET. The various circuits such as NOT, NAND, NOR, AND, OR, XOR and XNOR gates are designed using CNTFET. Basic functions such as adder, subtractor, mux, decoder etc. in CMOS technology are implemented by using generated symbols of PCNFET and NCNFET. Voltage threshold losing which occurred in passing high and low voltages in NMOSFET and PMOSFET, respectively results in such implementation. CNFET technology provides more efficient way to implement these functions in terms of delay, power consumption and area. Voltage threshold is proportional to the, so increasing the diagonal of nanotube results in decreasing the voltage threshold toward zero. Consequently, PCNFET and NCNFET could be utilized in designing various sequential circuits. They can even be utilized in designing ternary logic circuits.

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